Image s nsing apparatus provided with a plurality of automatic adjustments using common signal paths.

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Abstract

An image sensing apparatus includes: a signal processing circuit for processing image sensing signals; a plurality of adjustment signal generating circuits for generating mutually different signals for automatic adjustment by using part of the signals of the signal processing circuit; an interface for inputting the output of the plurality of adjustment signal generating circuits and outputting it through a common signal path; and a control microprocessor for adjusting a plurality of adjusting sections of the image sensing apparatus by using the output of the plurality of adjustment signal generating circuits output through the common signal path, wherein adjustment of the plurality of adjusting sections of the image sensing apparatus using the output of the plurality of adjustment signal generating circuits is effected with a reduced number of signal paths between the plurality of adjustment signal generating circuits and the control microprocessor, thereby simplifying the circuit construction of the image sensing apparatus as a whole and improving the reliability thereof.

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(54) Image sensing apparatus provided with a plurality of automatic adjustments using common signal paths.

(57) An image sensing apparatus includes: a signal processing circuit for processing image sensing signals; a plurality of adjustment signal generating circuits for generating mutually different signals for automatic adjustment by using part of the signals of the signal processing circuit; an interface for inputting the output of the plurality of adjustment signal generating circuits and outputting it through a common signal path; and a control microprocessor for adjusting a plurality of adjusting sections of the image sensing apparatus by using the output of the plurality of adjustment signal generating circuits output through the common signal path, wherein adjustment of the plurality of adjusting sections of the image sensing apparatus using the output of the plurality of adjustment signal generating circuits is effected with a reduced number of signal paths between the plurality of adjustment signal generating circuits and the control microprocessor, thereby simplifying the circuit construction of the image sensing apparatus as a whole and improving the reliability thereof.

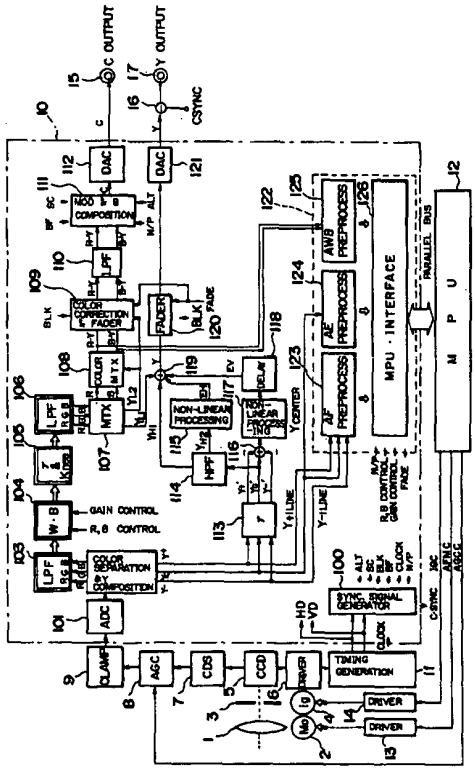

FIG. 1

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BACKGROUND OF THE INVENTION

Field of th Invention

The present invention relates to an image sensing apparatus and, in particular, to an image sensing apparatus which is suitable for circuit integration resulting from the digitization of signal processing operations in such an image sensing apparatus.

Related Background Art

There have been remarkable developments in the field of image sensing apparatuses, such as video cameras. The performance of such apparatuses has been improved and enhanced in various ways, for example, by equipping them with a number of functions. Further, a digital signal processing operation has recently been introduced into this field.

In this regard, an image sensing apparatus has already been proposed in which an output from an image sensing device, such as a two-dimensional CCD having minute color separation filters arranged over the entire surface thereof, is digitized by means of an AD converter, and subjected to a signal processing operation by a signal processing circuit using a digital processing technique, thereby obtaining television signals.

Further, integration of such image sensing apparatuses has been considered.

In the prior-art technique described above, however, the circuits for automatically effecting the focusing, exposure adjustment, white balance adjustment, etc. of the image sensing apparatus are controlled separately through different signal paths by means of a microcomputer, with the result that the construction of the image sensing apparatus as a whole is rather complicated. Further, in the prior-art technique, the number of IC chips used is rather large and, moreover, it is hard to integrate these IC chips. These factors have been a barrier to reducing the size of the image sensing apparatus as a whole. In such an image sensing apparatus, the digital signal processing is separately performed in different sections of the apparatus. Thus, it has been impossible to realize a digital integrated circuit for video cameras which is capable of synthetically performing signal processing operations in a digital video camera.

SUMMARY OF THE INVENTION

The present invention has been made with a view toward solving the problems mentioned above. It is a first object of the pres nt invention to provide an imag sensing apparatus in which a plurality of signal processing operations in the apparatus are simplified, and in which the number of signal paths is substantially reduc d, thereby simplifying the construction of the control syst m and improving th reliability of the imag s nsing apparatus.

A second obj ct of th present invention is to provid an image sensing apparatus in which an adjustment on adjusting sections related to an image sensing operation using the output of various adjustment signal generating means in the image sensing apparatus can be performed with substantially simplified signal paths between the adjustment signal generating means and the control means.

To achieve these objects, there is disclosed in accordance with a preferred embodiment of the present invention, an image sensing apparatus comprising:

signal processing means for processing image sensing signals;

a plurality of adjustment signal generating means for generating mutually different signals for automatic adjustment by using part of the signals of the signal processing means;

interface means for inputting the output of the plurality of adjustment signal generating means and outputting it through a common signal path; and

control means for adjusting a plurality of adjusting sections of the image sensing apparatus by using the output of the plurality of adjustment signal generating means output through the common signal path.

A third object of the present invention is to provide an image sensing apparatus in which the signal paths between the control means and a plurality of signal processing blocks for performing various signal processing operations of the image sensing apparatus and the signal processing operations are simplified, thereby making it possible to realize a one-chip-type control circuit for controlling an image sensing operation.

A fourth object of the present invention is to provide an image sensing apparatus in which it is possible to use a semiconductor device of a small mounting area having a substantially reduced number of output terminals, thereby improving the reliability of the image sensing apparatus.

A fifth object of the present invention is to provide an image sensing apparatus in which adjustment of a plurality of adjusting sections of an image sensing apparatus by means of the output of the plurality of adjustment signal generating circuits can be performed with substantially reduced signal paths between a plurality of adjustment signal generating circuits and a control microprocessor, thereby simplifying the circuit construction of the image sensing apparatus as a whole and improving the reliability thereof.

To achi v these obj cts, there is disclosed in accordanc with a pref rred embodiment of the pr - sent invention, an image s nsing apparatus comprising the following compon nts which are integrat d on a common semiconductor:

signal processing means for processing image sensing signals;

a plurality of adjustment signal generating means for generating mutually different signals for automatic adjustment by utilizing part of the signals of the signal processing means; and

interface means for inputting the output of the plurality of adjustment signal generating means and outputting it through a common signal path.

A sixth object of the present invention is to provide an image sensing apparatus in which various adjusting circuits of the image sensing apparatus are adapted to perform digital signal processing operations, and in which the control system for these signal processing circuits is simplified, thereby realizing a one-chip microprocessor for image sensing apparatuses.

A seventh object of the present invention is to provide a digital signal processing circuit IC for video cameras in which digital signal processing circuit blocks for automatic focusing, white balance adjustment, and automatic iris adjustment are realized in a one-chip structure.

An eighth object of the present invention is to provide a digital signal processing circuit interface for video cameras in which interface blocks for outputting parameters for performing adjustments regarding an image sensing operation, such as automatic focusing, white balance adjustment and automatic iris adjustment to a common arithmetic circuit are realized in a one-chip structure.

Other objects and features of the present invention will become apparent from the following embodiments and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is diagram showing an embodiment of the present invention;

Fig. 2 is a detailed diagram illustrating an AF preprocessing in the embodiment of Fig. 1;

Fig. 3 is a diagram illustrating the case where the AF frame of Fig. 2 is enlarged;

Fig. 4 is a diagram illustrating the case where the AF frame of Fig. 2 is reduced;

Fig. 5 is a detailed diagram illustrating an AE preprocessing in the embodiment of Fig. 1;

Fig. 6 is a diagram illustrating a centralized AE photometric distribution in Fig. 5;

Fig. 7 is a diagram illustrating a counter-light measurement frame in Fig. 5;

Fig. 8 is a detailed view of an AWB pre-process in the embodiment of Fig 1;

Fig. 9 is a diagram illustrating an AWB frame in Fig. 8;

Fig. 10 is a detailed view of an MPU interface in the embodiment of Fig. 1;

Fig. 11 is a flowchart illustrating the operation of an MPU in the embodiment of Fig. 10 when power is turned on;

Fig. 12 is a diagram illustrating the operation when an interrupt due to VD has occurred in the MPU operation flowchart of the embodiment of Fig. 10;

Fig. 13 is a diagram illustrating an operation of AF control in step 612 of the operation flowchart of Fig. 12;

Fig. 14 is a diagram illustrating an operation of AE control in step 613 of the operation flowchart of Fig. 12;

Fig. 15 is an operation diagram illustrating a continuation of the operation flowchart of Fig. 14;

Fig. 16 is a diagram illustrating counter-light detecting operations in steps 640 to 642 of the operation flowcharts of Figs. 14 and 15;

Fig. 17 is a diagram illustrating a frame C for AE control in Fig. 12;

Fig. 18 is an operation diagram illustrating an AWB control in step 614 of the operation flowchart of Fig. 12;

Fig. 19 is an operation diagram showing a continuation of the operation flowchart of Fig. 18; and

Fig. 20 is a diagram illustrating an AWB frame in Fig 19.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[First Embodiment]

Fig. 1 is a block diagram illustrating an embodiment of the present invention.

Numeral 1 indicates an image sensing lens; numeral 2 indicates an automatic focusing (AF) motor for rotating a focus ring of the image sensing lens 1; numeral 3 indicates a diaphragm; numeral 4 indicates an IG meter for controlling the aperture of the diaphragm 3; and numeral 5 indicates a two-dimensional color image sensing device including minute color separating filters (hereinafter referred to as "CCD"). However, the image sensing device of the present invention is not restricted to CCD; it is also possible to employ an image pickup tube or an X-Y address sensor. Numeral 6 indicates a CCD driver for driving the CCD 5; numeral 7 indicates a correlative double sampling circuit (CDS) for removing clocks and reset noise from the photoelectric conversion output of the CCD 5; numeral 8 indicates an automatic gain control amplifier (AGC) for amplifying the output of the CDS 7 in accordance with a control signal AGCC; numeral 9 indicates a clamp circuit for fixing the black level of an input voltage to a fixed voltage; numeral 10 indicates an integrated circuit for performing signal processing operations on the output signals of the CCD supplied thereto to form predetermined color video signals; numeral 12 indicates a microprocessor unit (MPU)

which r ceiv s digital data on th signals supplied from the integrated circuit 10, controls th integrat d circuit 10 and, furth r, generates signals for controlling the AF motor 2, th IG meter 4, and th AGC 8; numeral 13 indicates an AF driver circuit for driving the AF motor 2; numeral 14 indicates an IG driver circuit for driving the IG meter 4; numeral 15 indicates a chrominance signal (C) output terminal; and numeral 16 indicates a luminance signal (Y) output terminal.

Numerals 100 to 126 indicate inner circuit components of the integrated circuit 10, of which numeral 100 indicates a synchronization signal generator which generates a blanking pulse BLK, a burst flag pulse BF, a color sub-carrier SC, a line sequential signal ALT, a composite synchronization signal CSYNC, etc. for the generation of standard television signals, in response to a clock pulse, a horizontal synchronization pulse HD and a vertical synchronization pulse VD which are supplied from a timing generation circuit 11, an NTSC and a PAL switching signal N/P which are supplied from the MPU 12, and clock pulses of different frequencies needed for the interior of the integrated circuit 10.

Numeral 101 indicates an AD converter for generating digital signals in accordance with input signals. The circuits from this AD converter onward treat digital signals. Numeral 102 indicates a color-separation/luminance signal-synthesis circuit which includes two delay lines of one horizontal line, a matrix circuit and a switching circuit and which is adapted to separate color signal components R, G and B from input signals and to synthesize a luminance signal Yc, and further, to synthesize luminance signals Y- and Y+ which are vertically shifted by one line upwardly and downwardly from Yc. Numeral 103 indicates a low-pass filter for effecting band restriction and time-division sampling; and numeral 104 indicates a white balance (WB) circuit for varying the gains of time-divided color channels.

Numeral 105 indicates a gamma & Knee circuit for performing gamma correction and level compression of high-luminance components; numeral 106 indicates a low-pass filter which receives time-division signals to convert them to continuous parallel signals of three channels (R, G and B) and which further effects band restriction; numeral 107 indicates a matrix circuit which synthesizes low-band luminance signals YL1 and YL2 from R, G and B; numeral 108 indicates a color difference matrix circuit for generating signals R-Y and B-Y from R, B and YL2; numeral 109 indicates a color correction circuit for performing gain control over the color-difference signals and including a color correction matrix; numeral 110 indicates low-pass filter; and numeral 111 indicat s a modulation circuit which adds up the color-differenc signals after modulating them by a color sub-carrier (SC) and which furth r adds a color burst signal.

Num rals 112 and 121 indicate DA convert rs for converting digital signals to analog signals; numeral 113 indicat s a gamma-correction circuit for p rforming gamma correction on the thr e luminanc signals input; numeral 114 indicates a high-pass filt r which only passes predetermined high-luminance components of the luminance signals; numeral 115 and 117 indicates non-linear processing circuits which compress those input signals which are around the zero level; numeral 118 indicates a delay line for effecting delay corresponding to the delay time of the high-pass filter 114; numeral 119 indicates an adder; and numeral 120 indicates a fader for changing the gains of the luminance signals and performing blanking processing.

Numeral 122 indicates a preprocessing section which performs processing such that the delivery of data to and from the MPU and the processing by the MPU are facilitated when the MPU reads those signals of the different sections of the integrated circuit 10 which are necessary for control operations, such as automatic focusing (AF), automatic exposure control (AE) and automatic white balance control (AWB). The circuits indicated by numerals 123 to 126 are provided in the preprocessing section 122. An AF preprocessing circuit 123 performs preprocessing of AF; an AE preprocessing circuit 124 performs preprocessing of AE; an AWB preprocessing circuit 125 performs preprocessing of AWB; and an MPU interface circuit 126 delivers the output of these preprocessing circuits to the MPU 12, and receives control data on the different sections of the integrated circuit 10 supplied from the MPU 12.

Next, the operation of the above embodiment will be described. An image of a subject (not shown) is adjusted in terms of quantity of light by the image sensing lens 1 and diaphragm 3, and is transmitted through the above-mentioned minute color separation filters of the CCD 5 to undergo color separation. Then, the image is formed on the photoelectric conversion surface of the CCD to undergo photoelectric conversion pixel by pixel, and output sequentially as image sensing signals in response to the driving pulses of the driver circuit 6. First, the clock components and reset noise are removed from these image sensing signals by the CDS circuit 7, and the signals are amplified by the AGC circuit 8 in accordance with the gains corresponding to the AGCC signals. The black level is fixed to a reference voltage which is substantially at the lower limit of the input range of the ADC circuit 101, and the signals are converted to digital signals by the AD converter 101 in the integrated circuit 10.

These digital signals are first separated into color compon nts of R, G and B by th color s paration/Y-synthesis circuit 102. At th same time, the luminance signal YC is synthesized along with the luminance signal Y-, which is on horizontal line abov (b fore) this luminanc signal, and the luminanc signal Y+, which

is one horizontal line below (after) this luminance signal. Thes R, G and B signals are restrict d to a fixed band by the low-pass filter 103, and th n thre -phase-convert d to time-division signals to become on -channel signals. In the WB circuit 104, these signals are amplified in accordance with fixed gains set by the MPU 12. In this process, white balance adjustment is effected by changing only the gains of the R and B signals, and, by simultaneously varying the gains of the R, G and B signals, an overall gain control can be effected.

This output is subjected to gamma correction and high-luminance-component compression by the gamma & Knee circuit 105, and is restored to the R, G and B signals by the low-pass filter 106. After being restricted to a fixed band, the R, G and B color signals are added up at a fixed ratio by the matrix circuit 107 to form low-pass luminance signals YL1 and YL2. As stated below, YL1 is subjected to re-sampling at the same sampling rate as a high-pass luminance signal so as to form a high-pass luminance signal. YL2 is not subjected to re-sampling since it is only used for the formation of color difference signals.

Subtraction is performed on the YL2, R and B at a fixed ratio by the color difference matrix circuit 108 to form color difference signals R-Y and B-Y. These color difference signals are subjected to gain control, predetermined matrix computation and color correction by the color-correction/fader circuit 109. Further, when the MPU 12 designates a fading operation, a gradual gain variation is effected. This output is subjected to re-sampling by the low-pass filter 110 at a sampling rate needed for color modulation, for example, four times the frequency of the color subcarrier SC, restricted to a fixed band, and modulated at the modulation circuit 111 by the color sub-carrier SC, with a burst signal being superimposed in accordance with a burst flag signal BF. If, at this time, the N/P signal designates PAL, the burst signal and chrominance signal are inverted in a fixed phase in accordance with the ALT signal so as to be adapted to the PAL standard.

This output is digital-analog converted by the DA converter 112 and output from a C-output terminal 15 as a chrominance signal to be supplied to a VTR, television monitor or the like (not shown).

The luminance signals Yc, Y- and Y+, output from the color-separation/Y-synthesis circuit 102, are subjected to gamma correction by the gamma correction circuit 113 to form, first, high-pass luminance signals YH1 and YH2 by means of the high-pass filter 114. Here, it is assumed that the signal YH1 is beyond the band of the low-pass luminance signal YL1 for generating the above-mention d luminanc signal, and that th range of th signal YH2 is 3 to 4MHz or more, etc.

The signal YH2 is converted by the non-lin ar processing circuit 115 to a horizontal contour emphasis signal EH which has undergone compression around the zero level. Th output of the gamma correction circuit 113 is subject d to addition and subtraction by the adder 116 and is likewis subjected to compression around the zero level by the non-linear processing circuit 117, and delayed by the delay circuit 118 to become a vertical contour emphasis signal EV. The signals YL1, YH1, EH and EV are added up by the adder 119 to form a luminance signal Y, which is subjected to blanking processing by the fader 120, and, as in the above case, a gradual gain variation is effected at the time of the fading operation.

The output signal is digital-analog converted by the DA converter 121 and added to the composite synchronization signal CSYNC by the adder 16, and is output from a Y-output terminal 17 to be supplied, as in the above-described case, to a VTR, television monitor or the like (not shown).

The signals Yc, Y- and Y+ are processed by the AF preprocessing circuit 123 to form requisite data for AF, and the signal Yc is processed by the AE preprocessing circuit 124 to form requisite data for AE. Further, the output signals R-Y and B-Y from the above-described color difference matrix circuit 108 are processed by the AWB preprocessing circuit 125 to form requisite data for AWB. These items of data are read by the MPU circuit 12 through the MPU interface circuit 126.

Fig. 2 shows in detail the AF preprocessing circuit 123 of Fig. 1. Numeral 201 indicates an adder; numerals 202 and 206 indicates absolute value circuits for obtaining the absolute values of input signals; numerals 203 and 207 indicate gate circuits for gating input signals in accordance with a gate signal SG1; numerals 204 and 208 indicate maximum value hold circuits for holding the maximum values of input signals; numeral 205 indicates a band pass filter; numeral 209 indicates an AF frame register for retaining the position and size of an AF frame on an image plane; numeral 210 indicates a comparator; numeral 211 indicates an H counter which is reset by a horizontal synchronization signal HD to count clocks; numeral 212 indicates a V counter which is reset by a vertical synchronization signal VD to count HD; and numeral 213 indicates an internal bus for connecting the AF preprocess circuit 123, the AE preprocess circuit 124 and the AWB preprocess circuit 125 to the MPU interface circuit 126.

First, the H counter 211 and the V counter 212 generate a signal corresponding to the present scanning position of an image sensing signal in the image plane, and the signal is compared by the comparator 210 with frame data previously written to the AF frame register 209 to generate a fram signal SG1 repr -senting the AF frame, i. ., the extraction rang of th image s nsing signal for AF.

A high-frequency-band component ranging, e.g., from 1 to 3MHz, which is r quired for AF, is xtract d

from the input luminance signal Yc by th band pass filter 205, and th absolute value th reof is obtained by the absolute value circuit 206 to be gat d by th gat circuit 207 in accordanc with th abov -m ntioned gate signal SG1 within the range corresponding to the above-mentioned AF frame, the maximum value hold circuit 208 holding the maximum value EH of the high-frequency component in the horizontal direction in the above AF frame.

In this process, an AF reset signal B is generated, for example, during vertical blanking interval, by the MPU interface circuit 126, thereby resetting the maximum value hold circuit 208. Afterwards, the maximum value EH held by the maximum value hold circuit 208 is output to the internal bus 213 due the generation of an AF read signal B at the beginning of the next vertical blanking interval.

Further, in the adder 201, addition and subtraction are performed on the luminance signals Yc, Y- and Y+, to obtain a high-pass component in the vertical direction, which is converted to an absolute value by the absolute value circuit 202, and gated by the gate circuit 203 in accordance with the above-mentioned gate signal SG1, and the maximum value EV of the high-frequency component in the vertical direction within the AF frame is held by the maximum value hold circuit 204.

As in the case of the maximum value hold circuit 208, the operations of resetting and reading out to the internal bus 213 of the data being held are performed in accordance with an AF reset signal A and an AF read-out signal A, respectively.

The maximum values in the horizontal and vertical directions of the high-frequency component thus read out are used in AF control in accordance with the algorithm shown in Fig. 13.

Figs. 3 and 4 illustrate the AF frame of Fig. 2. In the drawings, the outer frame represents an image plane, and the inner frame represents the AF frame. When, for example, coordinate values x1, y1, x2 and y2 are written to the AF register 209 in the manner shown in Fig. 3, the AF frame obtained is relatively large with respect to the image plane, and when coordinate values x3, y3, x4 and y4 are written in the manner shown in Fig. 4, the AF frame obtained is relatively small with respect to the image plane. Switching between the two manners of writing is effected by a switch SW1 of Fig. 10 described below. The pattern of the AF frame is not restricted to that of this embodiment. Further, it is also possible for a plurality of AF frames to exist simultaneously.

Fig. 5 shows in detail the AE preprocess circuit 124 of Fig. 1. Numeral 301 indicates a gate circuit for s tting an AE frame in th image plan ; num rals 302, 304 and 305 indicate integrators; numeral 303 indicates a switching circuit; numeral 306 indicates a C-frame register; numeral 307 indicates a comparator; numeral 308 indicates an H count r which is reset by HD and adapted to count clocks; num ral 309 indicates V counter which is res t by VD and adapt d to count clocks; and numeral 310 indicates a d coder for gen rating a pr det rmin d frame signal.

First, a signal corresponding to the scanning position of the image sensing signal in the image plane is generated by the H counter 308 and the V counter 309, and this signal is compared by the comparator 307 with C-frame data previously written to the C-frame register from the MPU interface circuit 126 by an AE-frame-C-register writing pulse, thereby generating a frame signal SG2. At the same time, the output of the H counter 308 and that of the V counter 309 are input to the decoder 310 to form a predetermined frame signal SG3.

The input luminance signal Yc is first gated by the gate circuit 301 in accordance with the gate signal SG2 of a movable frame, and is integrated by the integrator 302. At this time, an AE reset signal C is generated by the MPU interface circuit 126, for example, during the vertical blanking interval, thereby resetting the integrator 302. When an AE read-out signal C is generated by the MPU interface circuit 126 at the beginning of the next vertical blanking interval, data which has been integrated by the integrator 302 is output to the internal bus 213.

Further, the luminance signal Yc is switched by the switching circuit 303 in accordance with the gate signal SG3 of a predetermined frame, and is integrated by the integrator 304 or 305.

At this time, as in the above-described case, the resetting of the integrators 304 and 305 and data output are effected in accordance with the AE reset signals A and B and the AE read-out signals A and B.

Figs. 6 and 7 are diagrams illustrating the operation of the circuit shown in Fig. 5. In the drawings, the outer frame represents the image plane. In Fig. 6, the portion on the outside of the frame represented by predetermined coordinate values (X1, Y1) and (X2, Y2) is referred to as area A, and the portion on the inside of the same is referred to as area B, the luminance signals in these areas being respectively input to the integrators 304 and 305 shown in Fig. 5. When coordinate values (x5, y5) and (x6, y6) are written to the C-frame register 306, a C-frame as shown in Fig. 7 is obtained, and the luminance signal on the inside of the frame is input to the integrator 302 shown in Fig. 5.

The output of the integrators 302, 304 and 305 thus read out are used in AE control in accordance with the algorithm shown in Figs. 14 to 17 described below. The pattern of the AE frame is not restricted to the above described; the position, number, combination, etc. th r of may b changed as ne ded.

Fig. 8 shows in d tail the AWB preprocess circuit 125 of Fig. 1. Numerals 401 and 403 indicate gat circuits for s tting an AWB frame; numerals 402 and 404 indicate integrators; numeral 405 indicate an AWB

frame register; numeral 406 indicates a comparator; numeral 407 indicat s an H counter which is r set by HD and adapt d to count clocks; and numeral 408 indicates a V counter which is res t by VD and adapted to count HD.

First, the H counter 407 and the V counter 408 generate signals corresponding to the scanning position of the image sensing signal in the image plane, and these signals are compared by the comparator 406 with AWB-frame data written to the AWB frame register 405 from the MPU interface circuit 126 in accordance with AWB-frame-register writing pulses., thereby generating a gate signal SG4.

The input color difference signals R-Y and B-Y are first gated by the gate circuits 401 and 403 in accordance with the AWB frame gate signal SG4, and are integrated by the integrators 402 and 404. During, for example, the vertical blanking interval, R-Y reset signal and B-Y reset signal are generated by the MPU interface circuit 126, and the integrators 402 and 404 are reset. At the beginning of the next blanking interval, R-Y read-out signal and B-Y read-out signal are generated, and integrated data is output to the internal bus 213.

Fig. 9 illustrates the operation of the circuit shown in Fig. 8. The outer frame portion represents the image plane. When coordinates (x7, y7) and (x8, y8) are written to the AWB frame register 405, an AWB frame as shown in the drawing is obtained, and the color difference signals on the inside of this frame are input to the integrators 402 and 404 of Fig. 8.

The output of these integrators 402 and 404 is used in AWB control in accordance with the algorithm shown in Figs. 18 to 20 described below.

Fig. 10 shows in detail the MPU circuit 12 and the MPU interface circuit 126 of Fig. 1. The components indicated by numerals 501 to 509 are provided inside the MPU circuit 12. Numeral 501 indicates a CPU circuit; numeral 502 indicates a memory for holding predetermined programs and data; numeral 503 indicates an internal bus of the MPU circuit; numerals 504 and 505 indicate DA converters; numerals 506, 507 and 508 indicate I/O ports; and numeral 509 indicates an interruption generating section. Numerals 510 and 511 indicate switches connected to the I/O port 506 of the MPU circuit 12; numerals 512 and 513 indicate bus buffers adapted to operate in accordance with control signals; and numeral 514 indicates a command decoder adapted to interpret input commands and generate signals for controlling the different sections inside the integrated circuit 10.

In accordance with the program of the memory 502, the CPU 501 reads the conditions of the switches SW1 and SW2 conn cted to the IO port 506, inputs and outputs data and commands to the MPU interfac circuit 126 through IO ports 507 and 508, and generates an AF motor control voltage AFMC and an IG control voltage IGC through the DA converters 504 and 505. Further, when th v rtical synchronization signal VD is input, the int rruption generating section 509 g nerates in th CPU 501 an interruption signal, whereby the CPU performs proc ssing at th time of interruption.

The switch SW1 is a switch for setting the size of the AF frame. By manipulating this switch, the operator can select either of the AF frames having different sizes shown in Figs. 3 and 4. Further, it is also possible to employ an arrangement in which still other patterns can be selected. The switch SW2 is a switch for performing a fading operation. By depressing this switch, the operator can effect fade-out or fade-in of an image. The command decoder 514 receives a command from the IO port 507 in accordance with a chip select signal CS generated at the IO port 508, and interprets the command. When it is a write command, the bus buffer 512 is operated and, at the same time, a corresponding write pulse is generated. When it is a readout command, the bus buffer 513 is operated and, at the same time, a corresponding read-out pulse is generated.

Further, in accordance with a reset command, setting commands for different sections, etc., a reset pulse, an NTSC/PAL switching pulse, a fade signal, etc. are generated.

Figs. 11 to 19 are flowcharts illustrating the operation of the MPU circuit 12 shown in Fig. 10.

Fig. 11 shows the operation when power is turned on. The operation is started in step 601, and, in step 602, the NTSC/PAL switching is set, and the fixed values in the integrated circuit, such as the initial gain values, etc. are set through the MPU interface circuit 126. In step 603, the maximum value or integral value of each of the preprocess circuits for AF, AE and AWB is reset, and, in step 604, the initial value of each frame register is set. In step 605, interruption by the vertical synchronization signal VD is permitted, and, in step 606, the circuit goes into hold state. Afterwards, the operation is performed in accordance with the interruption due to VD.

Fig. 12 shows the operation at the time of VD interruption. When, in step 607, VD interruption is generated, the maximum value and integral value of each of the preprocess circuits for AF, AE and AWB are read, and, in step 609, the value of each of the frame registers for AF, AE and AWB is updated. In step 610, the R and B gain control values are updated and, in step 611, the maximum value and integral value of each of them are reset. The operations of steps 608 to 611 are completed within the vertical blanking interval. In steps 612 to 614, AF control, AE control and AWB control are performed and, in step 615, the circuit goes into hold stat again to await VD interruption. Th operations of steps 607 to 615 are compl t d within one vertical blanking interval (16ms to 20ms).

Fig. 13 illustrates in d tail th AF control in step

612 of Fig. 12. First, the control is started in step 616 and, in step 617, the maximum value EV of the r ad high-frequency compon nt in the v rtical direction is compar d with the maximum value EH of the high-fr - quency component in the horizontal direction. When EH is larger than EV, the AF operation is performed by using the high-frequency component in the horizontal direction. For this purpose, EH is substituted for the current value of the high-frequency component, Enow, in step 618. When, in step 617, EV is larger than EH, EV is substituted for Enow so as to use the high-frequency component in the vertical direction.

In step 620, the change in the high-frequency component, Ed, is obtained by subtracting the previous high-frequency component Eold from the current high-frequency component Enow. Further, Enow is substituted for Eold. In step 621, Ed is compared with predetermined threshold values Eth and -Eth. When Ed is smaller than -Eth, it is to be assumed that the high-frequency component has been reduced, i.e., the focus point has moved in the opposite direction, due to the rotation of the AF motor, or that the focus point has been displaced despite the motor remaining still. Accordingly, a judgment is made in step 622 as to whether the AF motor control voltage is 0 or not. When it is 0, a predetermined value SAF is substituted for AFMC in step 624 so as to turn the AF motor. When AFMC is not 0 in step 622, the polarity of AFMC is inverted so as to move the focus point in the opposite direction.

When, in step 621, Ed is larger than -Eth and smaller than Eth, it is to be assumed that the image sensing apparatus is in focus, so that in step 625, AFMC is reduced to 0 to stop the AF motor. When, in step 621, Ed is larger than Eth, focus control is in the right direction, so that AFMC is left as it is.

In step 626, the AFMC voltage set in the manner described above is output from the DA converter 504 inside the MPU 12. In step 627, the condition of the switch SW1 of Fig. 10 is checked. If the switch is in the OFF position, the frame size is set large, as shown in Fig. 3, in step 628 and, when the switch is in the ON position, the frame size is set small, as shown in Fig. 4, in step 629, the AF control being terminated in step 630 to proceed to AE control.

Fig. 14 is a flowchart illustrating in detail the AE control in step 613 of Fig. 12. The control starts in step 631, and, in step 632, a weighting average AB of the areas A and B in Fig. 6 is obtained. That is, the integral value A of the area A obtained as the output of the integrator 304 of Fig. 5 is multiplied by a weight K1, and the integral value B of the area B obtained as the output of the integrator 305 of Fig. 5 is multiplied by a weight K2. By adding up th two int gral values, a weighting average AB is obtained. Furth r, the difference between this value and a ref rence value ABr is obtained as ABe.

In st p 633, the value of AB is multiplied by a predetermined coefficient K3, and the value thus obtain d is subtracted from the current IG driv voltage IGC, thereby obtaining the n xt IG driv voltag IGC.

In step 634, the integral signal C read from the integrator 302 of Fig. 5 is substituted for data Cij on the current position of the C-frame, and, in step 635, j is incremented by 1. In step 636, j is compared with a predetermined number of division in the horizontal direction, n. If j is smaller than or equal to n, the procedure advances to step 640; if it is greater than n, j is set to 1 in step 637, and i is incremented by 1.

Further, in step 638, i is compared with a predetermined number of division in the vertical direction, m. If i is smaller than or equal to m, i is left as it is, and, when it is greater than m, i is set to 1 in step 639. Then, in step 640, the minimum value of C in the area D of Fig 16, CDmin, is obtained, and, in step 641, the average of C in the area E of Fig. 16, CEavg, is obtained. In step 642 of Fig. 15, the ratio of CDmin to CEavg is compared with a predetermined threshold value Cth. When it is equal to or greater than Cth, the procedure advances to step 644; when it is smaller than Cth, the luminance of the background is rather high with respect to the subject, that is, the image sensing apparatus is in the so-called backlight state, so that, in step 643, a predetermined exposure correction value VBC is subtracted from IGC.

In step 604 of Fig. 11, the frame has been reset to C11, so that the frame C is sequentially switched field by field after power is turned on, with CDmin and CEavg changing each time such switching is effected.

In step 644, IGC is output from the DA converter 505. In step 645, x5, y5, x6 and y6 are obtained from the vertical and horizontal frame sizes a and b and the horizontal and vertical frame positions j and i so as to obtain the next position of the C-frame, and the AE control is terminated in step 646. Fig. 17 illustrates an AE control operation. In the drawing, the outer frame represents the image plane, which is divided into n sections in the horizontal direction and m sections in the vertical direction, the current position of the C-frame in the image plane being indicated by i and j. The AE control operation is terminated in step 646, and the procedure advances to AWB control.

Fig. 18 is a detailed flowchart of the AWB control step in Fig. 12. The AWB control is started in step 647, and, in step 648, the read data R-Y and B-Y is substituted for the color difference data on the current position of the AWB frame, (R - Y)ij and (B - Y)ij. In step 649, j is incremented by 1, and, in step 650, j is compared with the number of division in the horizontal direction of the AWB frame, n. When j is smaller than or equal to n, it is left as it is, and, if it is larger than n, j is set to 1 in step 651, and i is increm nted by 1. In step 652, i is compared with th number of division in th vertical direction of the AWB frame, m. Wh n i is small r than or qual to m, it is left as it is, and, if it is

larger than m, i is set to 1 in st p 653.

As in the case of the AE fram , the AWB frame is reset to the upper l ft corner of th image plane. Afterwards, it is shift d field by field.

In step 654, the weighting total SR-Y of (R - Y)ij is obtained, and, in step 655, the weighting total SB-Y of (B - Y)ij is obtained. If, in step 656, SR-Y is smaller than a predetermined threshold value -(R - Y)th, a predetermined value RGO is subtracted from the R gain control value RGAIN, in step 657. If, in step 656, SR-Y is greater than or equal to -(R - Y)th and smaller than or equal to (R - Y)th, the value is left as it is, and, if SR-Y is greater than (R - Y)th, the predetermined value RGO is added to RGAIN in step 658. Likewise, if, in step 659 of Fig. 19, SB-Y is smaller than a predetermined threshold value -(B - Y)th, a predetermined value BGO is subtracted from the B gain control value RGAIN, in step 660.

If, in step 659, SB-Y is greater than or equal to -(B - Y)th and smaller than or equal to (B - Y)th, the value is left as it is, and, if SB-Y is greater than (B - Y)th, the predetermined value BGO is added to BGAIN in step 661. In step 662, x7, y7, x8 and y8 are obtained from the vertical and horizontal frame sizes a and b and the horizontal and vertical frame positions j and i so as to obtain the next position of the AWB frame, and the AE control operation is terminated in step 663. The values of n, m, a and b in Fig. 18 may be the same as or different from those in Fig. 14. Fig. 20 illustrates an AWB frame. In the drawing, the outer frame represents the image plane, which is divided into n sections in the horizontal direction and m sections in the vertical direction, the current position of the AWB frame in the screen being indicated by i and j.

As described above, the present invention provides an image sensing apparatus comprising: signal processing means for processing image sensing signals; a plurality of adjustment signal generating means for generating mutually different signals for automatic adjustment by using part of the signals of the signal processing means; interface means for inputting the output of the plurality of adjustment signal generating means and outputting it through a common signal path; and control means for adjusting a plurality of adjusting sections of the image sensing apparatus by using the output of the adjustment signal generating means. Due to this construction, it is only necessary for the microprocessor to receive processed data when performing automatic focusing, automatic exposure adjustment, automatic white balance adjustment or the like. Accordingly, it is possible to adopt an inexpensive microprocessor having relatively limited processing capability. Further, since the processing op ration can be t rminat d within the vertical interval, the control sp ed can be increased. Furthermore, in the case wher an integrat d-circuit construction is adopt d, the number of circuits for conn ction with the microprocessor is small, so that the mounting ar a can be made very small, thereby making it possible to realize the imag sensing apparatus in a small size. Further, sinc no high-speed data is taken out of th integrated circuit, it is possible to minimize the radiation noise, the power noise due to capacity load and the like, thereby contributing to improvement in sensitivity.

Claims

1. An image sensing apparatus comprising:
   signal processing means for processing image sensing signals;
   a plurality of adjustment signal generating means for generating mutually different signals for automatic adjustment by using part of signals of said signal processing means;
   interface means for inputting an output of said plurality of adjustment signal generating means and outputting it through a common signal path; and
   control means for adjusting a plurality of adjusting sections of said image sensing apparatus by using the output of said plurality of adjustment signal generating means output through said common signal path.

2. An image sensing apparatus according to Claim 1, wherein said signal processing means, said adjustment signal generating means and said interface means are integrated on a common semiconductor.

3. An image sensing apparatus according to Claim 1, wherein said adjustment signal generating means generates signals for automatic focusing.

4. An image sensing apparatus according to Claim 1, wherein said adjustment signal generating means generates signals for automatic exposure adjustment.

5. An image sensing apparatus according to Claim 1, wherein said adjustment signal generating means generates signals for automatic white balance adjustment.

6. An image sensing apparatus comprising:
   signal processing means for processing image sensing signals;
   a plurality of adjustment signal generating means for generating mutually different signals for automatic adjustm nt by using part of signals of said signal processing means; and
   interface means for inputting an output of said plurality of adjustment signal generating means and outputting it through a common signal

path,

said signal processing means, said adjustment signal generating m ans and said int rface means being integrat d on a common semiconductor.

7. An image sensing apparatus according to Claim 6, wherein said adjustment signal generating means covers at least one of the following operations: automatic focusing, automatic iris adjustment and automatic white balance adjustment.

8. An image sensing apparatus according to Claim 7, wherein said interface means converts signals of said adjustment signal generating means to a common arithmetic-processing form.

9. An image sensing apparatus according to Claim 8, wherein said automatic focusing, said automatic iris adjustment and said automatic white balance adjustment are executed serially.

10. An image sensing apparatus comprising:
(A) image sensing means;
(B) extraction means for extracting predetermined signal components from image sensing signals output from said image sensing means to obtain a plurality of parameters for controlling an image sensing operation; and
(C) arithmetic processing means for computing control values on the basis of the plurality of parameters output from said extraction means; and
(D) interface means comprising preprocessing means adapted to convert said plurality of parameters to a form allowing arithmetic processing by said arithmetic processing means and mounted on a common integrated circuit.

11. An image sensing apparatus according to Claim 10, wherein said plurality of parameters are parameters for performing automatic focusing, automatic iris adjustment and automatic white balance adjustment.

12. An image sensing apparatus according to Claim 10, wherein said extraction means and said interface means are mounted on said common integrated circuit.

13. An image sensing apparatus according to Claim 10, wherein said interface means supplies an output from said pr processing means to said arithmetic processing means by m ans of a common bus.

14. An image s nsing apparatus according to Claim 10, wherein said interface means supplies an output from said preprocessing m ans to said arithmetic proc ssing means within a vertical interval of said image s nsing signals.

15. An image sensing apparatus according to Claim 14, wherein said arithmetic processing means terminates the arithmetic processing of control values within a vertical interval on the basis of output signals supplied from said interface means.

16. A signal processing circuit for video cameras, comprising:
(A) an extraction circuit for extracting a plurality of control parameters from image sensing signals output from image sensing means;
(B) a data conversion circuit for converting saidplurality of control parameters extracted by said extraction circuit to predetermined signal forms; and
(C) an output circuit for outputting an output from said data conversion circuit to a common bus.

17. A signal processing circuit according to Claim 16, further comprising a common arithmetic processing circuit for performing arithmetic processing serially on data output from said output circuit to generate control values corresponding to said control parameters.

18. A signal processing circuit according to Claim 17, further comprising an adjustment circuit for adjusting an image sensing operation in accordance with output control values of said arithmetic processing circuit.

19. A signal processing circuit according to Claim 18, wherein said adjustment circuit covers automatic focusing, automatic iris adjustment and automatic white balance adjustment.

20. A signal processing circuit according to Claim 16, wherein said extraction circuit, said data conversion circuit and said output circuit are mounted on a common semiconductor integrated circuit.

21. A camera control circuit comprising image sensing arrangements and camera control devices, an integrated signal processing circuit, and a relatively low speed microprocessor, microcomputer or microcontroller unit coupled to the signal processing circuit.

22. A camera control unit comprising a high spe d signal proc ssor and a low spe d microproc ssor

coupled to the signal processor, the signal processor performing the image processing and camera adjustment calculations and the microprocessor effecting relatively low speed control.

23. A digital signal processing circuit interface for video cameras, the interface being arranged to perform image processing and camera adjustment calculations, and to interface with a control unit.

FIG. 1

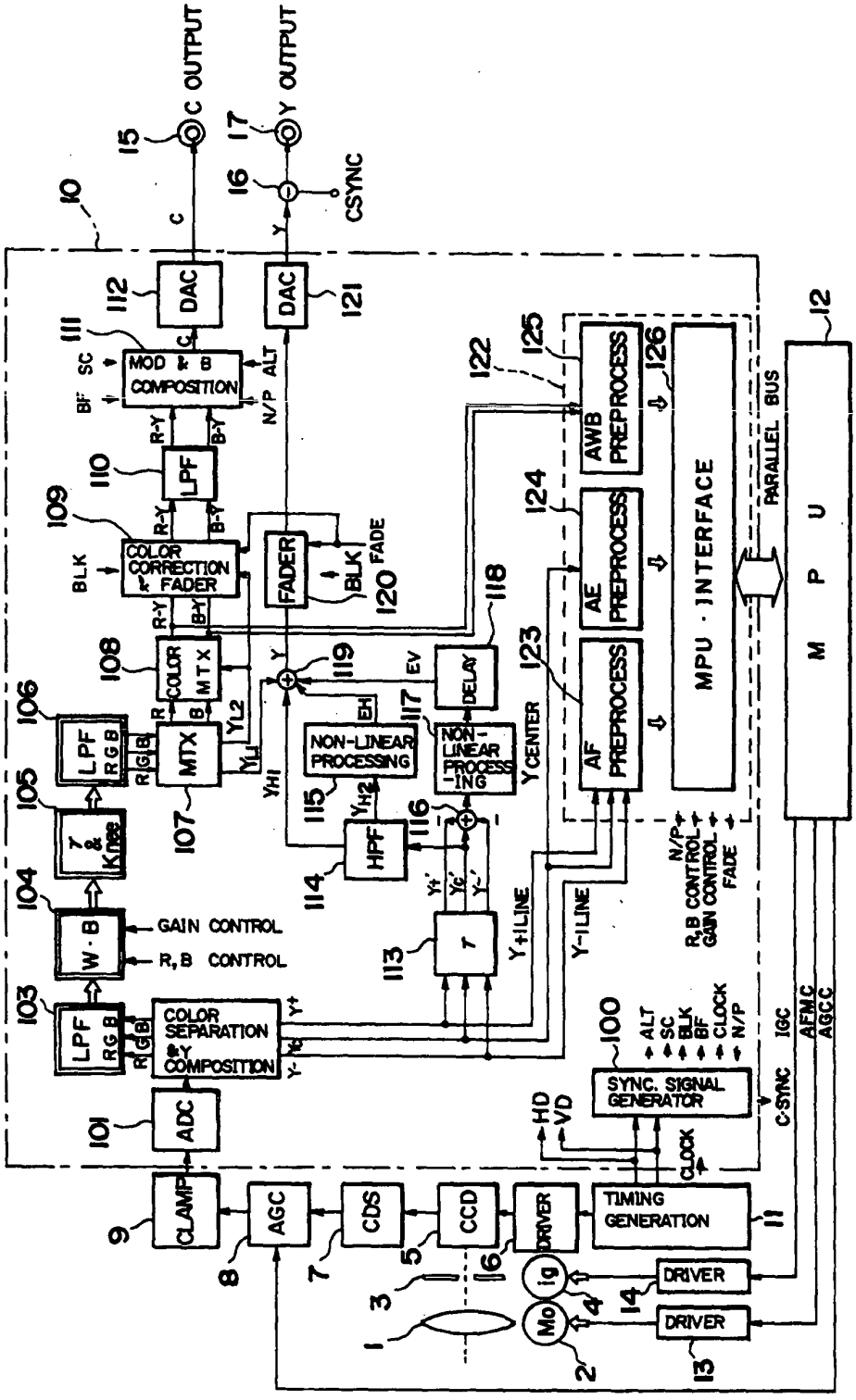

C OUTPUT
Y OUTPUT
CSYNC
DAC
DAC
MOD & B COMPOSITION
LPF
COLOR CORRECTION FADER
FADER
COLOR MTX
MTX
LPF
γ & Knee
W·B
GAIN CONTROL
R,B CONTROL
LPF
COLOR SEPARATION & Y COMPOSITION
ADC
CLAMP
AGC
CDS
CCD
DRIVER
TIMING GENERATION
DRIVER
DRIVER
NON-LINEAR PROCESSING
NON-LINEAR PROCESSING
DELAY
HPF
γ
Y+ILINE
Y-ILINE
AWB PREPROCESS
AE PREPROCESS
AF PREPROCESS
MPU · INTERFACE
PARALLEL BUS
M P U
SYNC. SIGNAL GENERATOR
HD
VD
CLOCK
C-SYNC
IGC
AFMC
AGCC
ALT
SC
BLK
BF
CLOCK
N/P
R,B CONTROL
GAIN CONTROL
FADE
BLK
FADE
EV
EH
YCENTER
TIMING GENERATION

FIG. 2

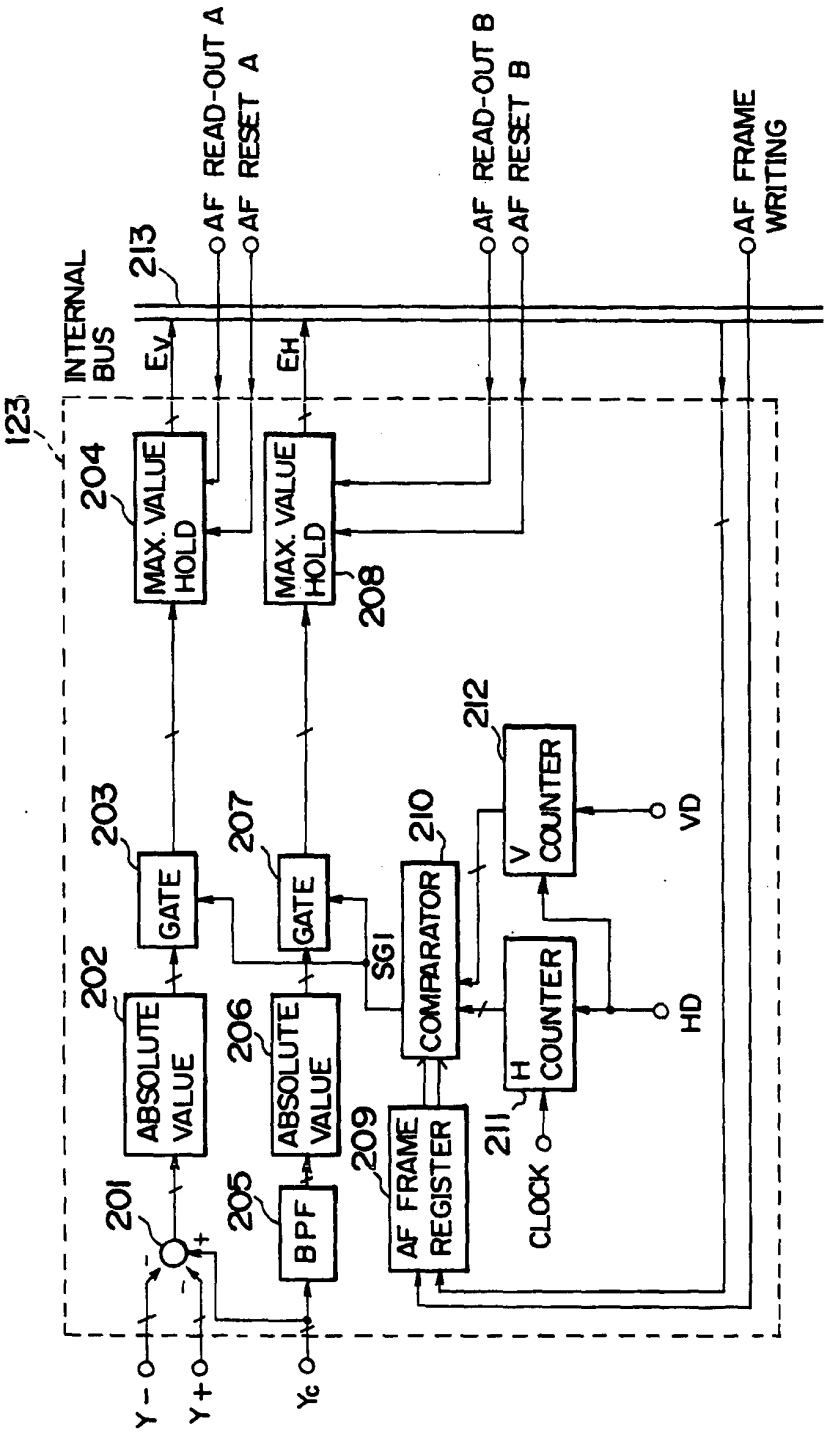

123
INTERNAL BUS
213
AF READ-OUT A
AF RESET A
AF READ-OUT B
AF RESET B
AF FRAME WRITING
Ev
EH
204
MAX. VALUE HOLD
208
MAX. VALUE HOLD
212
V COUNTER
VD
203
GATE
207
GATE
210
COMPARATOR
SG1
202
ABSOLUTE VALUE
206
ABSOLUTE VALUE
H COUNTER
HD
209
AF FRAME REGISTER
211
CLOCK
201
205
BPF
Y-
Y+
Yc

FIG. 3

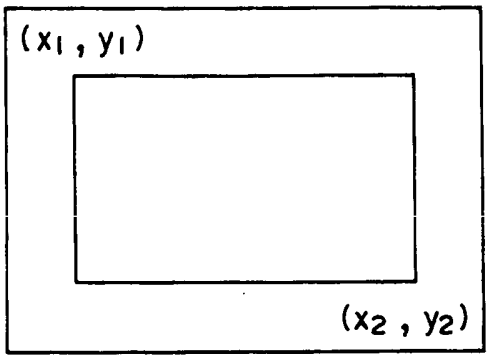


FIG. 4

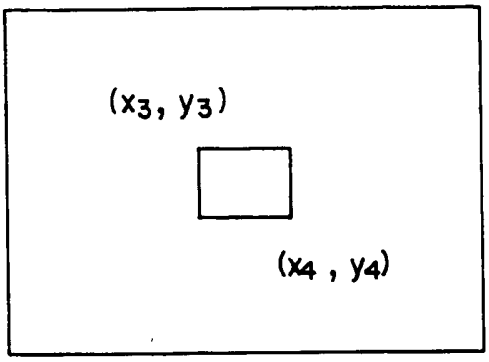


FIG. 5

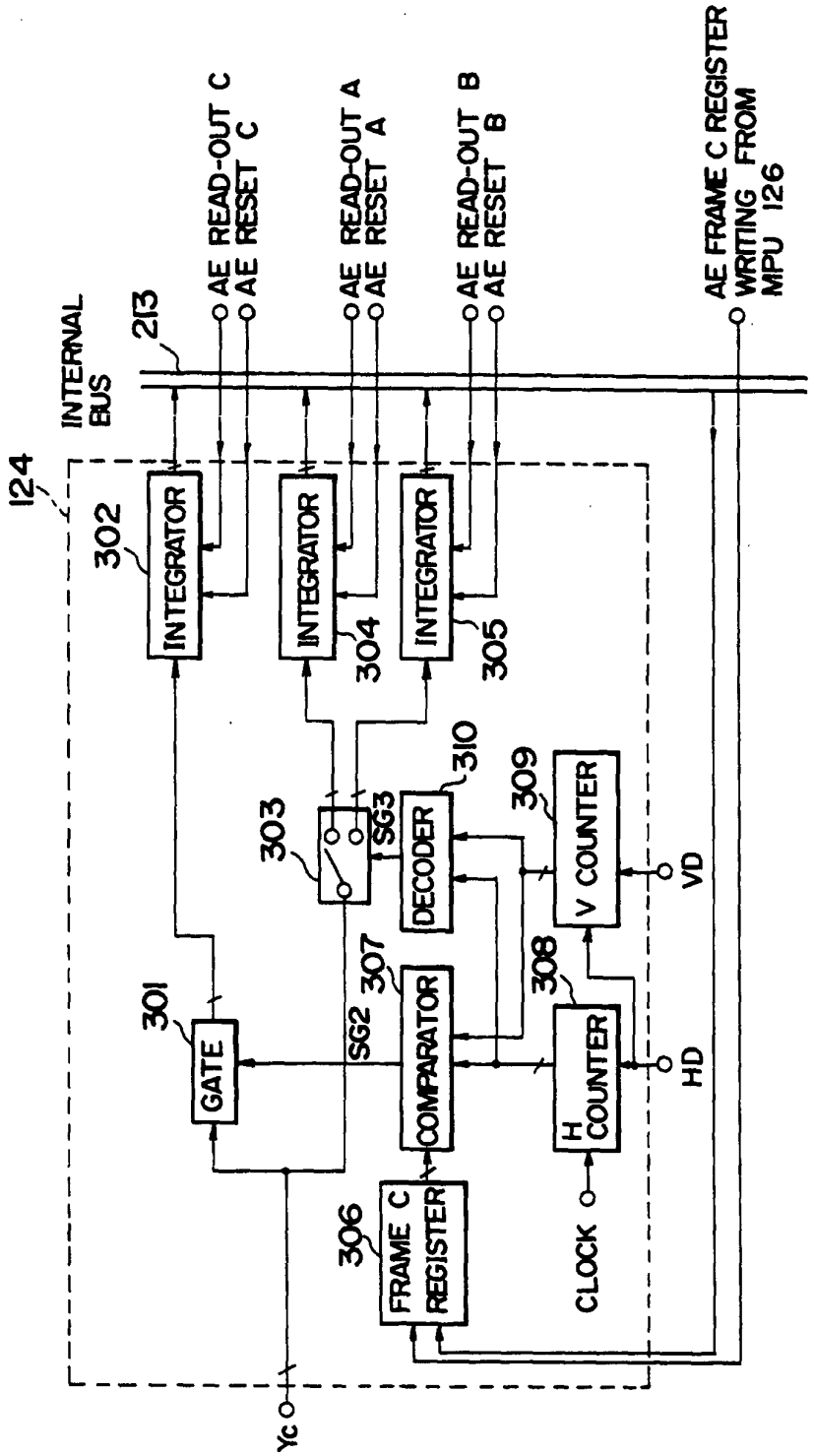

124
INTERNAL BUS
213
AE READ-OUT C
AE RESET C
AE READ-OUT A
AE RESET A
AE READ-OUT B
AE RESET B
AE FRAME C REGISTER WRITING FROM MPU 126
302
INTEGRATOR
304
INTEGRATOR
305
INTEGRATOR
303
SG3
310
DECODER
309
V COUNTER
VD
301
GATE
SG2
307
COMPARATOR
308
H COUNTER
HD
306
FRAME C REGISTER
CLOCK
Yc

FIG. 6

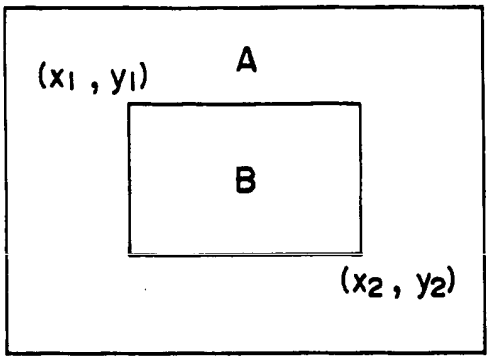


FIG. 7

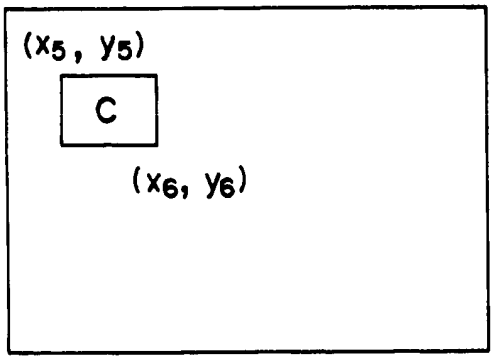


FIG. 8

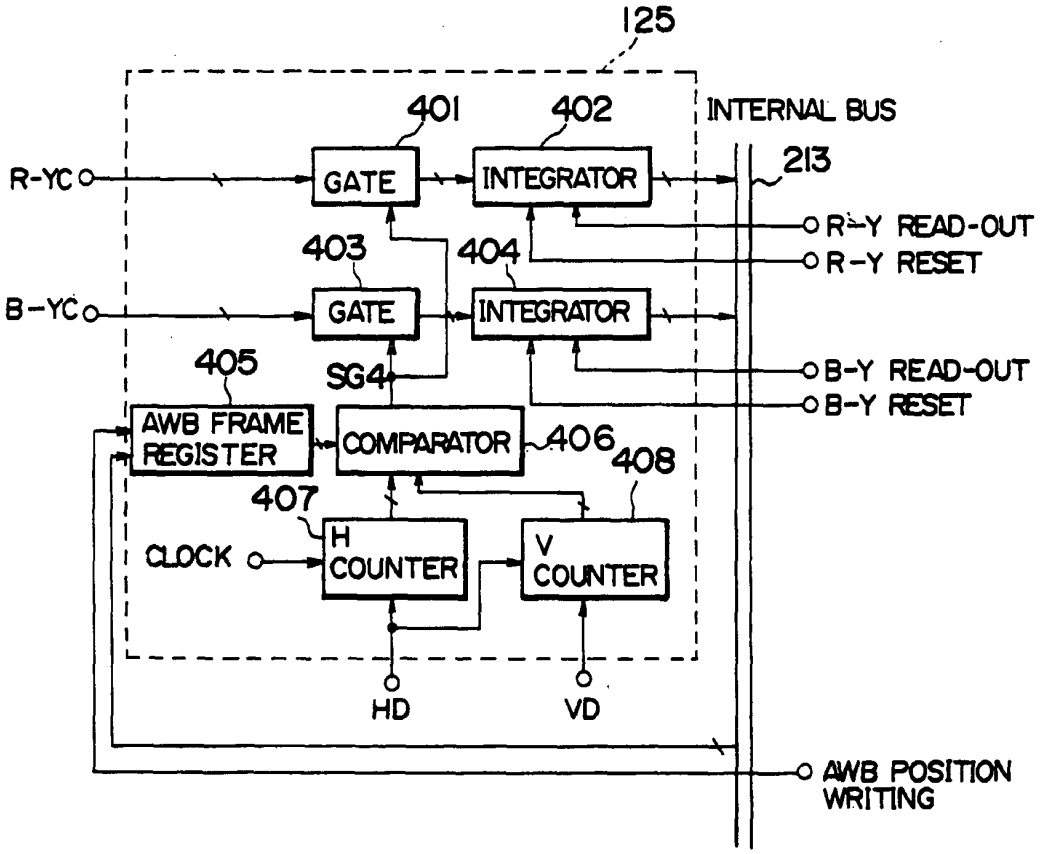

125
401
402
INTERNAL BUS
213
R-YC
GATE
INTEGRATOR
R-Y READ-OUT
R-Y RESET
403
404
B-YC
GATE
INTEGRATOR
405
SG4
B-Y READ-OUT
B-Y RESET
AWB FRAME REGISTER
COMPARATOR
406
408
407
CLOCK
H COUNTER
V COUNTER
HD
VD
AWB POSITION WRITING

FIG. 9

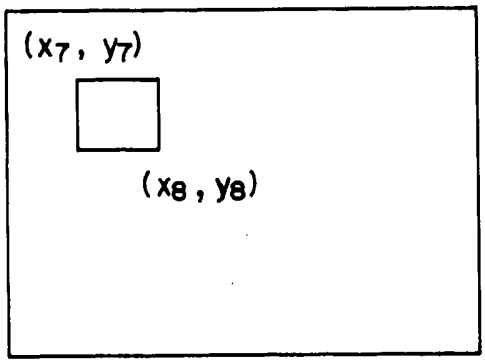


FIG. 10

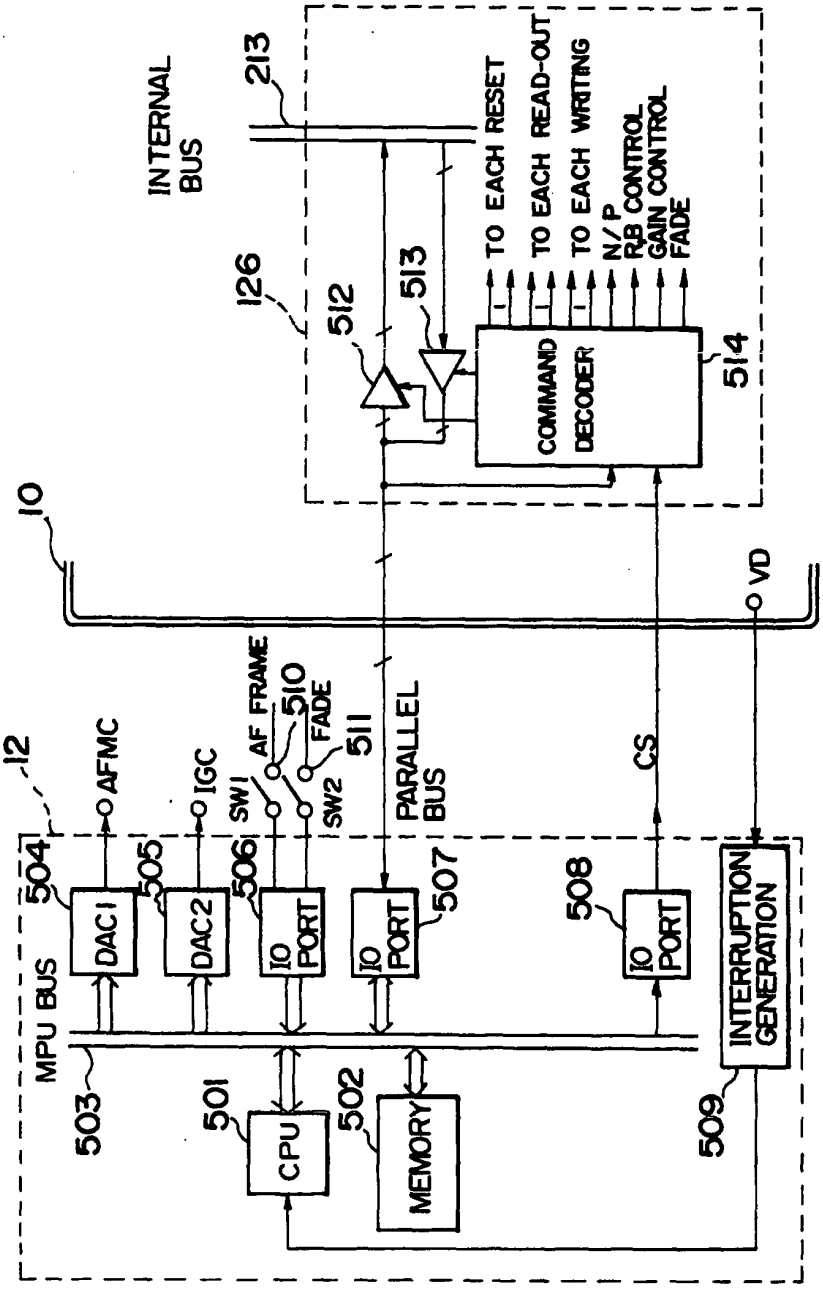

INTERNAL BUS
213
126
512
513
TO EACH RESET
TO EACH READ-OUT
TO EACH WRITING
N/P
R/B CONTROL
GAIN CONTROL
FADE
COMMAND DECODER
514
10
VD
12
AFMC
IGC
SW1
AF FRAME
510
FADE
SW2
511
PARALLEL BUS
CS
504
505
506
507
508
DAC1
DAC2
IO PORT
IO PORT
IO PORT
INTERRUPTION GENERATION
MPU BUS
503
501
502
509
CPU
MEMORY

FIG. 11

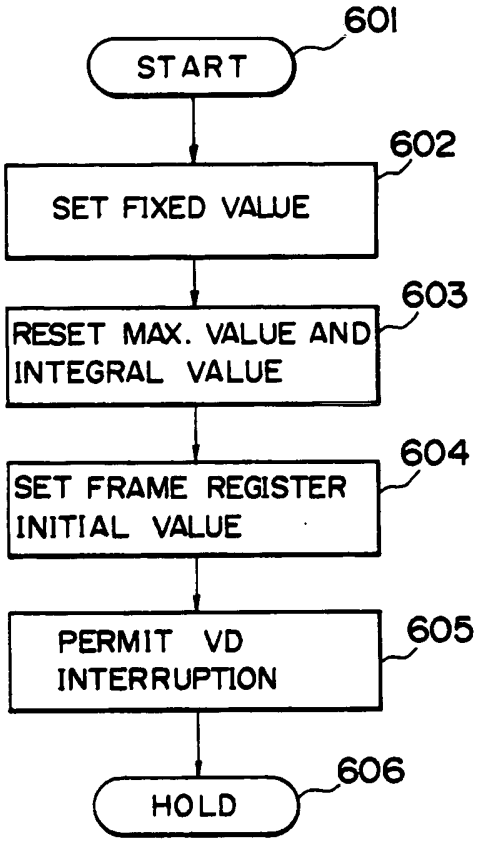

601
START
602
SET FIXED VALUE
603
RESET MAX. VALUE AND INTEGRAL VALUE
604
SET FRAME REGISTER INITIAL VALUE
605
PERMIT VD INTERRUPTION
606
HOLD

FIG. 12

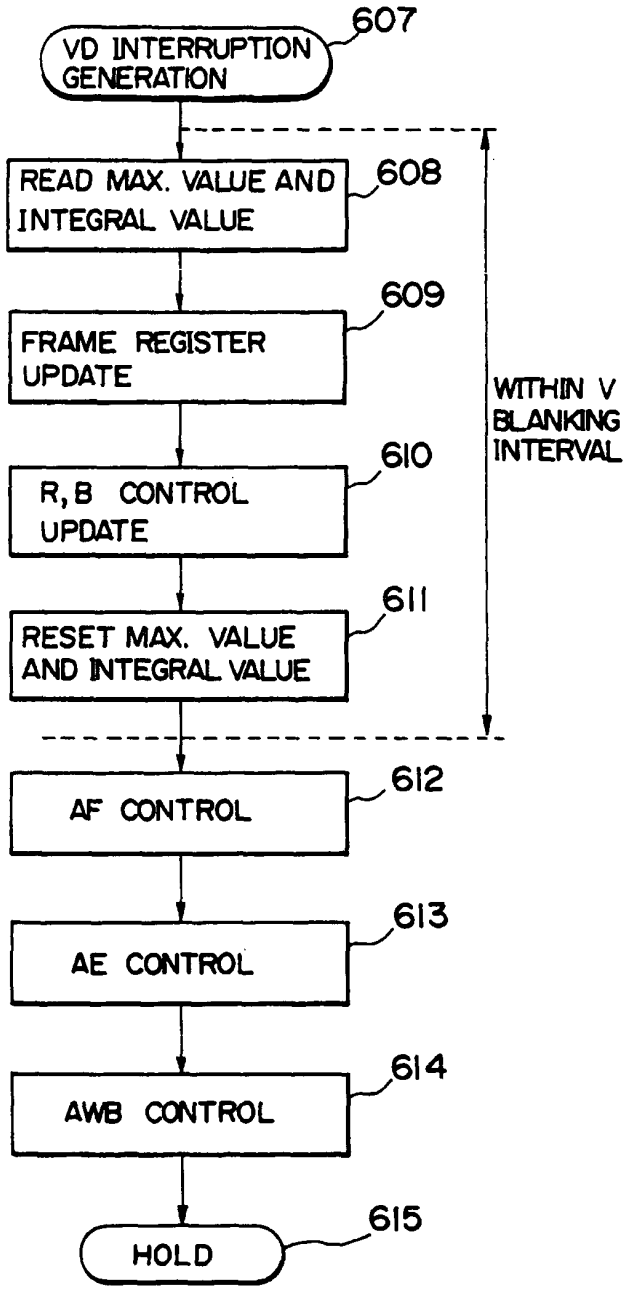

VD INTERRUPTION GENERATION
607
READ MAX. VALUE AND INTEGRAL VALUE
608
FRAME REGISTER UPDATE
609
R, B CONTROL UPDATE
610
RESET MAX. VALUE AND INTEGRAL VALUE
611
WITHIN V BLANKING INTERVAL
AF CONTROL
612
AE CONTROL
613
AWB CONTROL
614
HOLD
615

FIG. 13

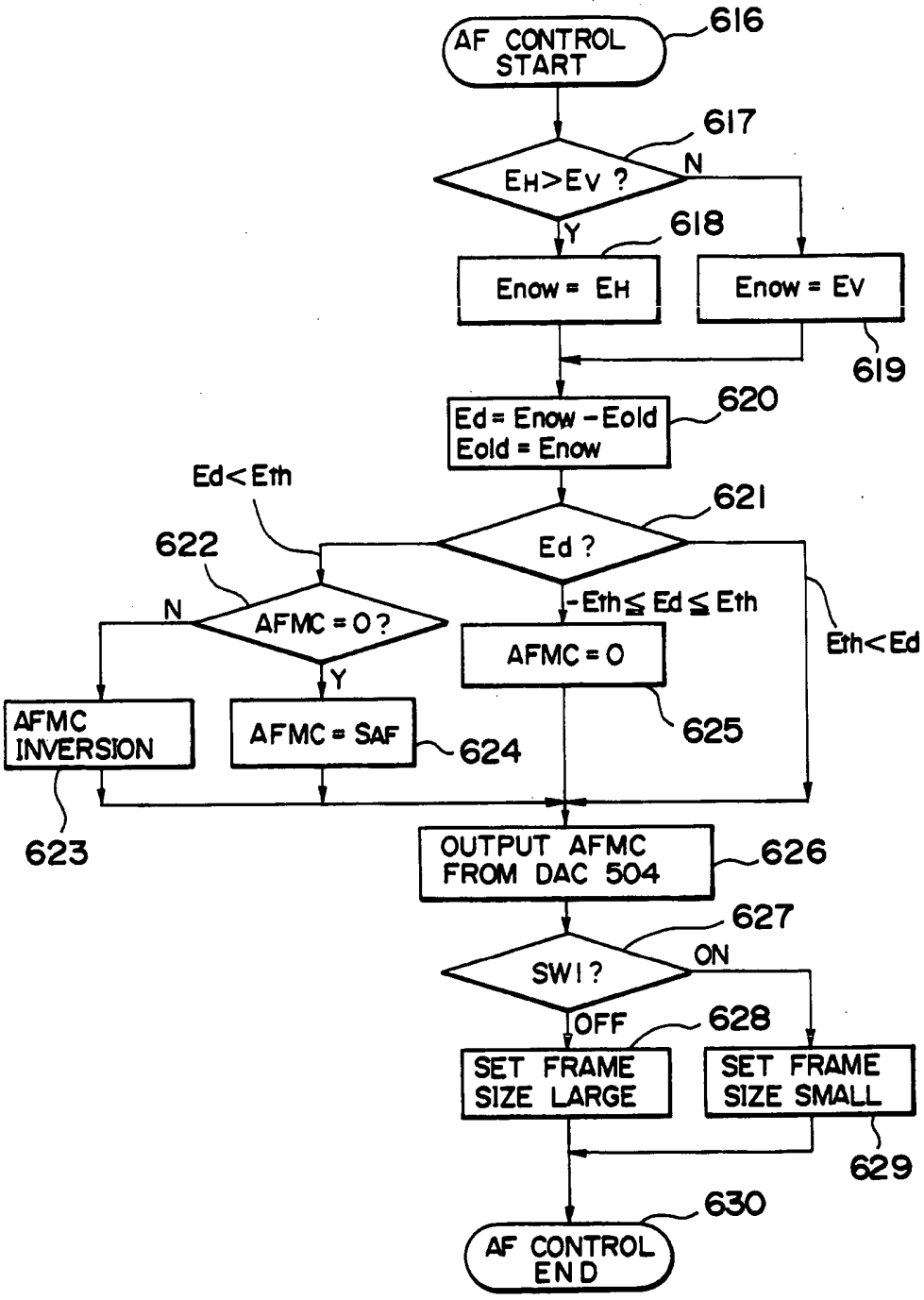

AF CONTROL START
616
617
EH>EV ?
N
Y
618
Enow = EH
Enow = EV
619
Ed = Enow - Eold
Eold = Enow
620
Ed<Eth
621
Ed ?
622
N
AFMC = 0 ?
Y
-Eth≦ Ed ≦ Eth
AFMC = 0
625
Eth<Ed
AFMC INVERSION
AFMC = SAF
624
623
OUTPUT AFMC FROM DAC 504
626
627
SW1 ?
ON
OFF
628
SET FRAME SIZE LARGE
SET FRAME SIZE SMALL
629
630
AF CONTROL END

FIG. 14

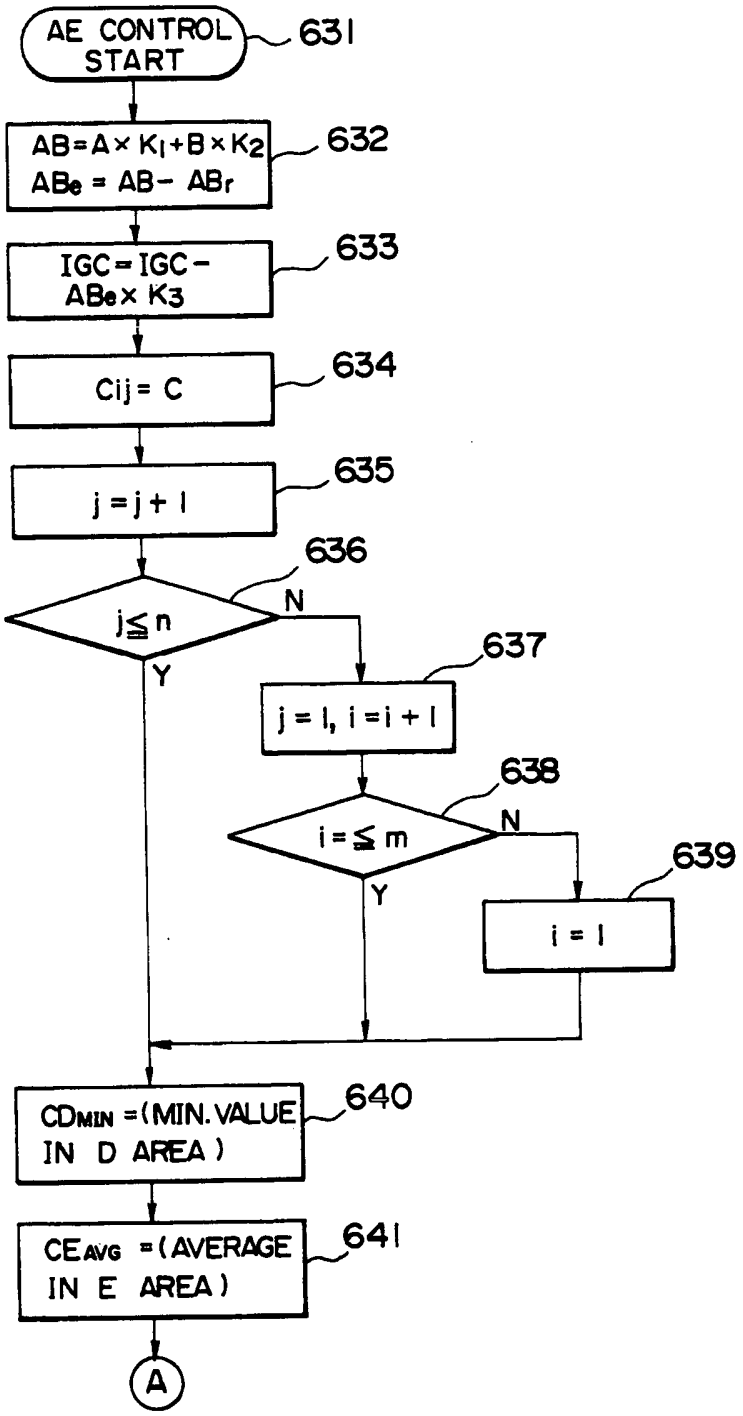

AE CONTROL START
631
AB=A×K1+B×K2
ABe = AB− ABr
632
IGC=IGC−ABe×K3
633
Cij = C
634
j = j + 1
635
636
j≦n
N
Y
637
j = 1, i = i + 1
638
i = ≦ m
N
Y
639
i = 1
CDMIN =(MIN. VALUE IN D AREA)
640
CEAVG =(AVERAGE IN E AREA)
641
A

FIG. 15

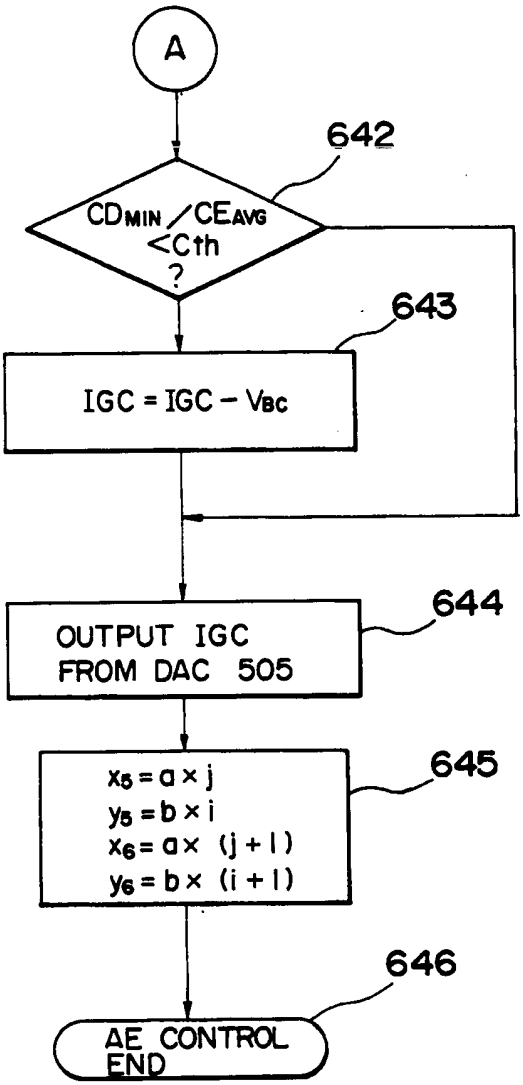

A
642
CDMIN / CEAVG <Cth ?
643
IGC = IGC − VBc
644
OUTPUT IGC FROM DAC 505
645
x5 = a × j
y5 = b × i
x6 = a × (j + 1)
y6 = b × (i + 1)
646
AE CONTROL END

FIG. 16

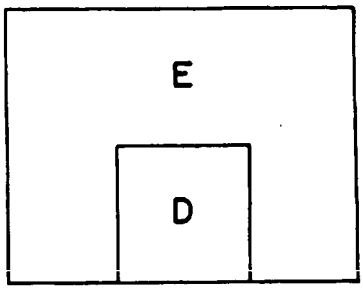
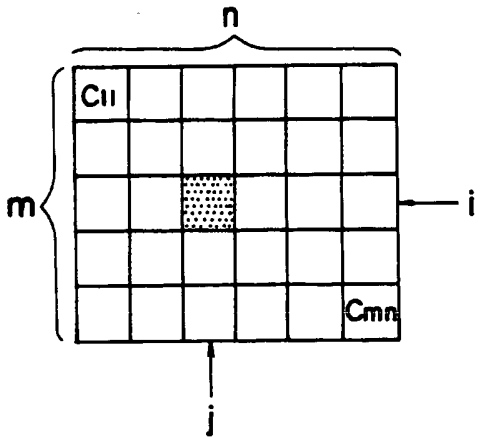


FIG. 17



DENOTE Cij

FIG. 18

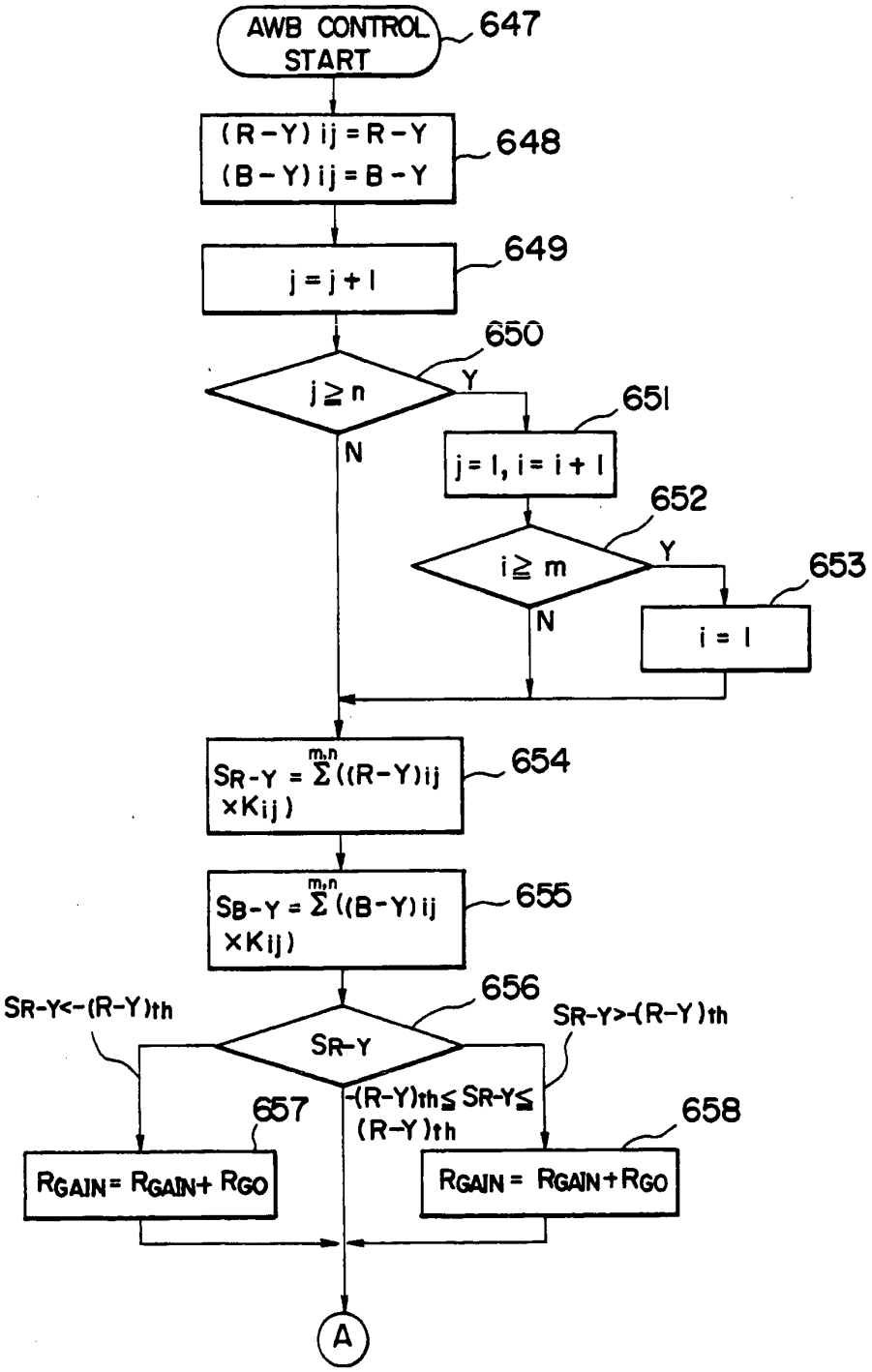

AWB CONTROL START
647
(R-Y) ij = R-Y
(B-Y) ij = B-Y
648
j = j + 1
649
650
j ≧ n
Y
N
651
j = 1, i = i + 1
652
i ≧ m
Y
N
653
i = 1
654
SR-Y = Σ m,n ((R-Y)ij ×Kij)
655
SB-Y = Σ m,n ((B-Y)ij ×Kij)
656
SR-Y
SR-Y<-(R-Y)th
SR-Y>-(R-Y)th
-(R-Y)th≦ SR-Y≦ (R-Y)th
657
RGAIN = RGAIN + RGO
658
RGAIN = RGAIN + RGO
A

FIG. 19

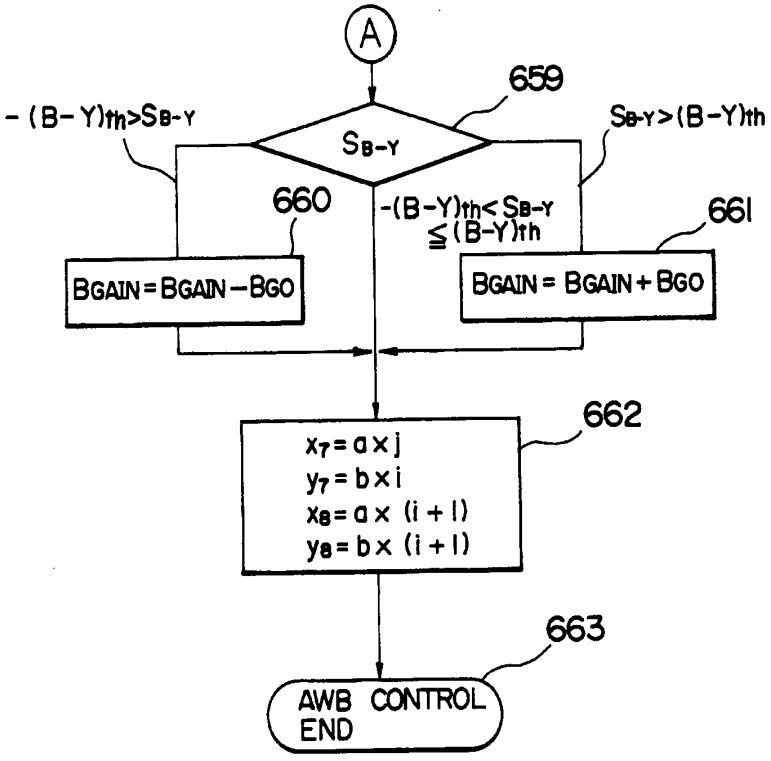
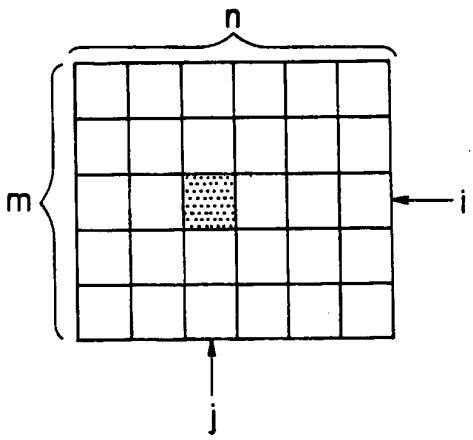

A
659
S_{B-Y}
$-(B-Y)_{th} > S_{B-Y}$
$S_{B-Y} > (B-Y)_{th}$
660
$-(B-Y)_{th} < S_{B-Y} \leqq (B-Y)_{th}$
661
BGAIN = BGAIN − BGO
BGAIN = BGAIN + BGO
662
$x_7 = a \times j$
$y_7 = b \times i$
$x_8 = a \times (i+1)$
$y_8 = b \times (i+1)$
663
AWB CONTROL END

FIG. 20



DENOTE $(R-Y)_{ij}$ AND $(B-Y)_{ij}$

(19) Europäisch s Pat ntamt
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(54) Image sensing apparatus provided with a plurality of automatic adjustments using common signal paths.

(57) An image sensing apparatus includes: a signal processing circuit (10) for processing image sensing signals; a plurality of adjustment signal generating circuits (123,124,125) for generating mutually different signals for automatic adjustment by using part of the signals of the signal processing circuit; an interface (1269 for inputting the output of the plurality of adjustment signal generating circuits and outputting it through a common signal path; and a control microprocessor (12) for adjusting a plurality of adjusting sections, like autofocussing, automatic exposure and/or automatic white balance, of the image sensing apparatus by using the output of the plurality of adjustment signal g nerating circuits output through the common signal path, wherein adjustment of the plurality of adjusting sections of the image s nsing apparatus using th output of the plurality of adjustment signal generating circuits is effected with a reduced number of signal paths between the plurality of adjustment signal generating circuits and the control microprocessor, thereby simplifying the circuit construction of the image sensing apparatus as a whole and improving the reliability thereof.

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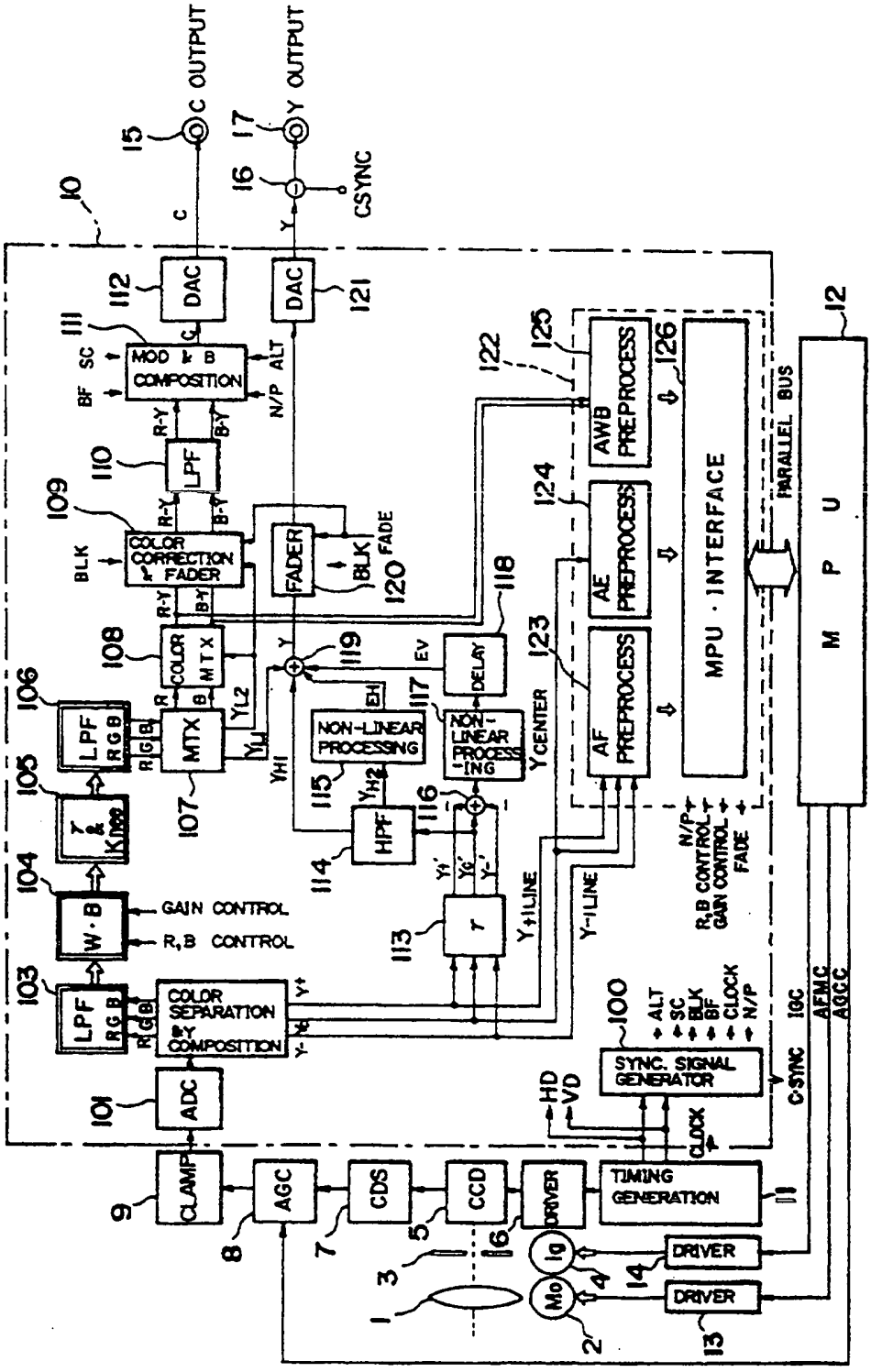
FIG. 1


C OUTPUT
Y OUTPUT
CSYNC
DAC
DAC
MOD COMPOSITION
LPF
COLOR CORRECTION FADER
FADER
COLOR MTX
MTX
LPF RGB
Y & K Data
W·B
GAIN CONTROL
R,B CONTROL
LPF RGB
COLOR SEPARATION COMPOSITION
ADC
CLAMP
AGC
CDS
CCD
DRIVER
TIMING GENERATION
DRIVER
DRIVER
NON-LINEAR PROCESSING
HPF
DELAY
NON-LINEAR PROCESSING
AWB PREPROCESS
AE PREPROCESS
AF PREPROCESS
MPU · INTERFACE
PARALLEL BUS
M P U
SYNC. SIGNAL GENERATOR
HD
VD
CLOCK
ALT
SC
BLK
BF
CLOCK
N/P
C-SYNC
IGC
AEMC
AGCC
R,B CONTROL
GAIN CONTROL
FADE
Y CENTER
Y+1LINE
Y-1LINE

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,X	EP-A-0 446 647 (SONY CORP.) * column 1, line 15 - line 28 * * column 6, line 35 - line 48 * * column 7, line 8 - line 50 * * column 8, line 7 - column 9, line 50 * * column 11, line 38 - column 12, line 19 * * column 12, line 41 - column 13, line 17 * * column 13, line 58 - column 14, line 42 * * column 15, line 42 - column 16, line 54 * * column 25, line 25 - line 30 * * column 27, line 31 - column 29, line 4 * * column 35, line 18 - line 42 * * column 36, line 31 - line 39 *	1,3-5, 16-19,23	H04N5/232 H04N5/235 H04N9/73
A		6-9,10, 11, 13-15, 21,22	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
Y	EP-A-0 356 123 (SONY CORP.) * column 2, line 45 - column 3, line 21 * * column 4, line 4 - line 15 * * column 6, line 5 - column 8, line 23 * * column 12, line 27 - line 50 *	1,5,16	H04N
A		3,4,6-8, 10,11, 18,10, 21-23	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 FEBRUARY 1993	DUHR R.H.J.E.

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	DE-A-3 320 690 (CANON K.K.) * page 12, line 32 - page 13, line 30 * * figure 4 *	1,5,16	
A	---	6,7,10,11,13,18,19,21-23	
A	US-A-4 814 861 (HIEDA) * column 3, line 46 - column 5, line 63 * * figure 2 *	1,2,6,10,12,16,20-23	
	-----		TECHNICAL FIELDS SEARCHED (Int. Cl.5)

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